IN THE CLAIMS

Please cancel claims 1-40 without prejudice.

Please add new claims 41-80 as follows:

1-40. (Cancelled)

41. (New) An electrical diagnostic circuit for the testing and/or the diagnostic analysis of an integrated circuit comprising:

a plurality of external inputs (E_n) for receiving digital values;

a plurality of essentially similar, series-connected switching units comprising:

each switching unit is connected to one external input for receiving a test signal of an integrated circuit;

each switching unit has an internal input for an input signal from a switching unit arranged upstream or downstream,

the switching units are configured to be controllable such that an input signal present at the internal input of a switching unit, in dependence on a control signal of the switching unit, are forwarded either unchanged to the internal input of the switching unit arranged downstream or to the circuit output and/or are fed back to an internal input of a switching unit arranged upstream, or are combined with the test signal in each case present at the external input and the combination value determined from this combination is forwarded to the internal input of the switching unit in each case arranged downstream or to the circuit output and/or is fed back to the internal input of a switching unit arranged upstream; and

a circuit output for outputting an output value.

42. (New) The electrical diagnostic circuit of claim 41, comprising wherein each

switching unit has one gate, comprising an exclusive OR gate, one multiplexer and one storage unit.

43. (New) The electrical diagnostic circuit of claim 42, comprising wherein each external input (E_n) leads to one input each of the exclusive OR gate, each internal input leading to one external input each of the multiplexer arranged downstream and, in parallel, to one second input each of the associated exclusive OR gate, each output of the exclusive OR gate leading to one second input each of the multiplexer and each output of the multiplexer leading to one input each of the storage element, the output of which represents the output of the switching unit.

44. (New) The electrical diagnostic circuit of claim 42, comprising wherein the internal input of at least one switching unit, in dependence on the control signal of the switching unit, is connected to the first input of the multiplexer or to the second input of the exclusive OR gate.

45. (New) The electrical diagnostic circuit of claim 41, comprising wherein the electrical diagnostic circuit has a controllable feedback unit , connected to the circuit output, which is constructed in such a manner that the output value is fed back to at least one internal input of a switching unit.

46. (New) The electrical diagnostic circuit of claim 45, comprising wherein the feedback unit is present as a controllable gate, particularly as a controllable AND gate and has a control signal input, the controllable gate being constructed in such a manner that the output value is be fed back to at least one internal input of a switching unit if a predetermined value is present at the control signal input.

47. (New) The electrical diagnostic circuit of claim 45, comprising wherein the switching

units of the electrical diagnostic circuit in each case have at least two, particularly series-connected storage units (D_1, D'_1; ...; D_n, D'_n), the output of the last storage unit (D'_1, ..., D'_n) in each case of each switching unit forming the output of the relevant switching unit.

48. (New) The electrical diagnostic circuit of claim 45, comprising wherein at least one further storage unit, not belonging to a switching unit, is provided which is connected to the output of a switching unit of the electrical diagnostic circuit.

49. (New) The electrical diagnostic circuit of claim 45, comprising wherein the feedback unit has an OR gate, particularly an exclusive OR gate, one input of the controllable gate being connected to the output of the OR gate and the inputs of the OR gate being formed by at least two feedback lines which in each case branch off after at least one switching unit and/or after in each case one storage unit.

50. (New) The electrical diagnostic circuit of claim 45, comprising wherein the feedback unit has a further controllable gate, particularly a controllable AND gate, a controllable OR gate, a controllable NAND gate or a controllable NOR gate, the inputs of the further controllable gate being formed by a further control signal input and by the output of the last switching unit, and the output of the further controllable gate forming the circuit output.

51. (New) The electrical diagnostic circuit of claim 45, comprising wherein at least one further gate, particularly an exclusive OR gate is provided which is in each case located between switching units arranged in series, the output value present at the circuit output being conducted to an input of this further gate.

52. (New) An electrical diagnostic circuit for the testing and/or the diagnostic analysis of an integrated circuit comprising:

a plurality of external inputs (E_n) for receiving digital values;

a plurality of essentially similar, series-connected switching units comprising:

each switching unit is connected to one external input for receiving a test signal of an integrated circuit;

each switching unit has an internal input for an input signal from a switching unit arranged upstream or downstream,

the switching units are configured to be controllable such that an input signal present at the internal input of a switching unit, in dependence on a control signal of the switching unit, are forwarded either unchanged to the internal input of the switching unit arranged downstream or to the circuit output and/or are fed back to an internal input of a switching unit arranged upstream, or are combined with the test signal in each case present at the external input and the combination value determined from this combination is forwarded to the internal input of the switching unit in each case arranged downstream or to the circuit output and/or is fed back to the internal input of a switching unit arranged upstream; and

a circuit output for outputting an output value comprising wherein the first switching unit has an AND gate and a storage unit and in that all further switching units have one gate each, particularly an exclusive OR gate (XOR_2 - XOR_n), one multiplexer each and one storage unit each.

53. (New) The electrical diagnostic circuit of claim 52, comprising wherein the first external input leads to the first input of the AND gate and a control line leads to the second input of the AND gate, the output of the AND gate leading to the storage unit, the output of which represents the output of the first switching unit, and in that each further external input in each case leads to one input of the in each case associated exclusive OR gate, each internal input of the switching units in each case leading to a first input of the downstream multiplexer and, in parallel, to a second input of the respective exclusive OR gate, each output of an exclusive OR gate in each case leading to a second input of the downstream multiplexer and each output of the multiplexer in each case leading to an input of the

downstream storage element, the output of which represents the output of the switching unit.

54. (New) The electrical diagnostic circuit of claim 53, comprising wherein for all switching units except the first switching unit, the internal input is connected to the first input of the multiplexer and to the second input of the exclusive OR gate.

55. (New) The electrical diagnostic circuit of claim 52, comprising wherein the output of the last switching unit is connected to a shift register with linear feedback.

56. (New) The electrical diagnostic circuit of claim 55, comprising wherein the shift register with linear feedback has an exclusive OR gate, a number of series-connected storage elements (D'_1, ..., D'_m) and at least one feedback line, which branches off after a storage element (D'_1, ..., D'_m) and which leads/lead to in each case one input of the exclusive OR gate, the first storage element (D'_1) being connected to the output of the exclusive OR gate.

57. (New) The electrical diagnostic circuit of claim 41, comprising wherein a selection circuit, which is intended for controlling the electrical diagnostic circuit, is provided at the inputs (E_n) of the electrical diagnostic circuit.

58. (New) The electrical diagnostic circuit of claim 41, that is integrated monolithically on the integrated circuit to be tested and/or to be diagnosed.

59. (New) A probe card for testing integrated circuits, the probe card having an electrical diagnostic circuit as claimed in one of claim 41.

60. (New) A load board for receiving a probe card for testing integrated circuits and/or with one or more test sockets for testing integrated circuits and/or for connecting a handler to a tester of integrated circuits, the load board having an electrical diagnostic circuit as claimed

in claim 41.

61. (New) A tester with measuring sensors, particularly for currents and voltages and with instruments for generating digital signals or datastreams, the tester having an electrical diagnostic circuit as claimed in claim 41.

62. (New) A method for testing and/or for the diagnostic analysis of an integrated circuit, comprising:

providing an electrical diagnostic circuit which has n external inputs for receiving test data of n parallel datastreams of an integrated circuit to be tested and/or to be diagnosed and which is capable of generating signatures from the received test data, the test data present at the n external inputs selectively being included or not included in the generation of the signatures,

connecting the electrical diagnostic circuit to the integrated circuit to be tested and/or to be diagnosed, in such a manner that the n inputs of the electrical diagnostic circuit are present at the n outputs of the integrated circuit;

controlling the switching units of the electrical diagnostic circuit in such a manner that the test data in each case present at the external inputs are included in the generation of the signatures;

detecting and processing the test data of the integrated circuit to be tested and/or to be diagnosed to form at least one signature in one or in more successive test runs through the electrical diagnostic circuit;

checking the signature for correctness by means of the test by comparing the signatures determined in the test with the correct signature stored in the tester or determined by the tester;

if at least one errored signature has been determined, carrying out the following processes:

performing k successive test runs, wherein in each case only those data, present at

the input E_i, of the n datastreams in the jth run are included in the compacting in the electrical diagnostic circuit if the binary coefficient $a_{i,j}$ of the equations for determining the control points of a linear separable error-correcting code with n information points u_1, ..., u_n and with k control points v_1, ..., v_k is equal to one, the k control points v_1, ..., v_k being determined by the k binary equations

$$v_1 = a_{1,1}\, u_1 \oplus \ldots \oplus a_{1,n} u_n$$

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$$v_1 = a_{k,1} u_1 \oplus \ldots \oplus a_{k,n} u_n$$

from the n information points.

Determining the errored elements in the n datastreams, particularly the errored scan cells of the diagnosed integrated circuit from the deviations of the observed output signatures output by the electrical diagnostic circuit at its output in the k test runs

$$[\, y_1^b, y_2^b, y_3^b, \ldots \,]$$

from the corresponding correct output signatures

$$[\, y_1^k, y_2^k, y_3^k, \ldots \,].$$

63. (New) The method of claim 62, comprising wherein the datastreams are data which are shifted out of the scan paths of an integrated circuit.

64. (New) The method of claim 62, comprising wherein the electrical diagnostic circuit is

an electrical diagnostic circuit as claimed in claim 41.

65. (New) The method of claim 62, comprising wherein the electrical diagnostic circuit is constructed on a probe card as claimed in claim 59, on a load board as claimed in claim60 or on a tester as claimed in claim 61.

66. (New) The method of claim 62, comprising wherein the switching units are activated by means of a control signal in such a manner that the input signals present at the internal inputs of the switching units are combined with the test data in each case present at the external inputs and that the combination values in each case determined from these combinations are forwarded to the internal inputs of the switching units in each case arranged downstream.

67. (New) The method of claim 62, comprising wherein all control signals $c_{i,j}$, $1 \leq i \leq k$, $1 \leq j \leq n$ of the multiplexers (MUX_1, ..., MUX_n) are selected to be one.

68. (New) The method of claim 62, comprising wherein if the electrical diagnostic circuit has a feedback unit, it is activated in such a manner that it does not feed back.

69. (New) The method of claim 62, comprising wherein if the electrical diagnostic circuit has a feedback unit, it is activated in such a manner that it does not feed back.

70. (New) The method of claim 62, comprising wherein performing successive test runs is carried out as follows:

carrying out k successive test runs, wherein a control point is determined with each run in accordance with the following rule from the information points until all control points (v_k) have been determined,

$$v_1 = a_{1,1}u_1 \oplus \ldots \oplus a_{1,n}u_n$$

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$$v_k = a_{k,1}u_1 \oplus \ldots \oplus a_{k,n}u_n$$

wherein the coefficients $a_{i,j}$ with $1 \leq i \leq k$, $1 \leq j \leq n$ assume the values zero or one, the switching units of the electrical diagnostic circuit being controlled in such a manner that the test data present at the jth external input in the ith run are only subjected to a combination in the switching units if the control signal $c_{i,j}$, with $1 \leq i \leq k$, $1 \leq j \leq n$, assumes the value one, whereby the control signal $c_{i,j}$ assumes the value zero if the associated coefficient $a_{i,j}$ assumes the value zero or if an indeterminate value in the datastream is to be blanked out.

71. (New) The method of claim 62, comprising wherein the value of the control signal present at the first input of the AND gate assumes the value zero if an indeterminate value is present at the output of the upstream storage element D_n, and thus at its second input.

72. (New) The method of claim 62, comprising wherein performing successive test runs is carried out as follows: carrying out k successive test runs by the switching units of the electrical diagnostic circuit being controlled in accordance with the binary coefficients $a_{i,j}$ of the equations for determining the control points v_1, ..., v_k of a linear separable error-correcting code with n information points u_1, ..., u_n and with k control points v_1, ..., v_k, in such a manner that the test data (u, t, s, r) present at the jth external input (E_j) in the ith run are only subjected to a combination in the switching units of the electrical diagnostic circuit when the binary control signal $c_{i,j}$, with $1 \leq i \leq k$, $1 \leq j \leq n$, assumes the value one, whereby the control signal $c_{i,j}$ assumes the value zero when the associated coefficient $a_{i,j}$ in the linear equations for determining the k control points of the error-detecting code assumes the value zero or when an indeterminate value in the datastream is to be blanked out, the k control

points v_1, ..., v_k being determined from the k binary equations

$$v_1 = a_{1,1}u_1 \oplus \ldots \oplus a_{1,n}u_n$$

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$$v_k = a_{k,1}u_1 \oplus \ldots \oplus a_{k,n}u_n$$

from the n information points.

73. (New) The method of claim 72, comprising wherein the multiplexers of the switching units are controlled by the control signals.

74. (New) The method of claim 72, comprising wherein a selection circuit which controls the input into the electrical diagnostic circuit is provided between the outputs (A_n) of the integrated circuit and the inputs (E_n) of the electrical diagnostic circuit.

75. (New) Using the method of claim 72 for testing and/or for the diagnostic analysis of printed board assemblies or of circuit boards.

76. (New) A computer program for carrying out a method for testing an integrated circuit comprising:

providing an electrical diagnostic circuit which has n external inputs for receiving test data of n parallel datastreams of an integrated circuit to be tested and/or to be diagnosed and which is capable of generating signatures from the received test data, the test data present at the n external inputs selectively being included or not included in the generation of the signatures,

connecting the electrical diagnostic circuit to the integrated circuit to be

tested and/or to be diagnosed, in such a manner that the n inputs of the electrical diagnostic circuit are present at the n outputs of the integrated circuit;

controlling the switching units of the electrical diagnostic circuit in such a manner that the test data in each case present at the external inputs are included in the generation of the signatures;

detecting and processing the test data of the integrated circuit to be tested and/or to be diagnosed to form at least one signature in one or in more successive test runs through the electrical diagnostic circuit;

checking the signature for correctness by means of the test by comparing the signatures determined in the test with the correct signature stored in the tester or determined by the tester;

if at least one errored signature has been determined, carrying out the following processes:

performing k successive test runs, wherein in each case only those data, present at the input E_i, of the n datastreams in the jth run are included in the compacting in the electrical diagnostic circuit if the binary coefficient $a_{i,j}$ of the equations for determining the control points of a linear separable error-correcting code with n information points u_1, ..., u_n and with k control points v_1, ..., v_k is equal to one, the k control points v_1, ..., v_k being determined by the k binary equations

$$v_1 = a_{1,1}\, u_1 \oplus \ldots \oplus a_{1,n} u_n$$

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$$v_1 = a_{k,1} u_1 \oplus \ldots \oplus a_{k,n} u_n$$

from the n information points.

Determining the errored elements in the n datastreams, particularly the errored

scan cells of the diagnosed integrated circuit from the deviations of the observed output signatures output by the electrical diagnostic circuit at its output in the k test runs

$$[y_1^b, y_2^b, y_3^b, \ldots]$$

from the corresponding correct output signatures

$$[y_1^k, y_2^k, y_3^k, \ldots].$$

77. (New) The computer program of claim 76, which is contained on a storage medium.

78. (New) The computer program of claim 76, which is transmitted on an electrical carrier signal.

79. (New) A data carrier comprising a computer program as claimed in claim 76.

80. (New) A method in which a computer program as claimed in claim 76 is downloaded from an electronic data network.